AMENDMENTS TO THE CLAIMS

Claims 1-45 are pending. Claims 1, 3, 5, 6, 14, 15, 19, 31, 32, 35, 39, and 43 have been amended. A complete list of claims is presented below:

Current Listing of Claims

1. (Currently amended) A method comprising:

~~packing a cache line of each of a plurality of read data returns into one or more packets;~~

~~splitting each of the one or more packets into a plurality of flits; and~~

receiving at a memory controller a first read data return and a second read data return from a first memory and a second memory, respectively;

splitting the first read data return into a first plurality of flits and the second read data return into a second plurality of flits;

interleaving the first and the second pluralities ~~plurality~~ of flits ~~of each of the plurality of read data returns~~ to be sent to a processor such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits.

2. (Original) The method of claim 1, further comprising sending the interleaved flits via a packetized interconnect.

3. (Currently amended) The method of claim 1, further comprising receiving the first and the second ~~plurality of~~ read data returns ~~from a plurality of memory channels~~ in a substantially overlapped manner.

4. (Original) The method of claim 3, wherein a critical chunk of an oldest read data return in a queue is sent in one or more first flits and a critical chunk of a second oldest read data return in the queue is sent in one or more second flits.

5. (Currently amended) The method of claim 3, further comprising:

adding a header to each of the first and the second ~~plurality of~~ read data returns; and

sending the header before each of the first and the second ~~plurality of~~ read data returns.

6. (Currently amended) An apparatus comprising:

a first buffer to temporarily hold a first cache line of a first read data return;

a second buffer to temporarily hold a second cache line of a second read data return; and

a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively,

such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits.

7. (Original) The apparatus of claim 6, further comprising an interface to output the interleaved flits in two packets.

8. (Original) The apparatus of claim 7, wherein the multiplexer time-multiplexes the first and the second pluralities of flits in a plurality of time slots to interleave the first and second pluralities of flits.

9. (Original) The apparatus of claim 8, wherein the multiplexer dynamically time-multiplexes the first and the second pluralities of flits.

10. (Original) The apparatus of claim 8, wherein the multiplexer statically time-multiplexes the first and the second pluralities of flits.

11. (Original) The apparatus of claim 7, wherein the interleaved flits are sent via a packetized interconnect to a processor.

12. (Original) The apparatus of claim 11, wherein a critical chunk of the first read data return is sent in one or more flits of the first plurality of flits and a

critical chunk of the second read data return is sent in one or more flits of the second plurality of flits.

13. (Original) The apparatus of claim 6, wherein a header is added to each of the first and second cache lines.

14. (Currently Amended) The apparatus of claim 11, wherein [[the]] a header is sent after the corresponding read data return starts arriving at one of the first and the second buffers.

15. (Currently Amended) The apparatus of claim 11, wherein [[the]] a header is sent before the corresponding-read data return starts arriving at one of the first and the second buffers.

16. (Original) The apparatus of claim 6, wherein the first and second read data returns arrive from a first memory channel and a second memory channel, respectively, in a substantially overlapped manner.

17. (Original) The apparatus of claim 6, further comprising:

a third buffer, coupled to the multiplexer, to temporarily hold a third cache line of a third read data return, wherein the multiplexer interleaves a third plurality of flits of the third cache line with the first and second pluralities of flits.

18. (Original) The apparatus of claim 17, further comprising:

a fourth buffer, coupled to the multiplexer, to temporarily hold a fourth cache line of a fourth read data return, wherein the multiplexer interleaves a fourth plurality of flits of the fourth cache line with the first, the second, and the third pluralities of flits.

19. (Currently amended) A system comprising:

a first plurality of dynamic random access memory ("DRAM") devices;

a second plurality of DRAM devices;

a DRAM channel coupled to the first plurality of DRAM devices;

a second DRAM channel coupled to the second plurality of DRAM devices; and

a memory controller coupled to the first and second DRAM channels, the memory controller including

a first buffer to temporarily hold a first cache line of a first read data return from the first DRAM channel;

a second buffer to temporarily hold a second cache line of a second read data return from the second DRAM channel; and

a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines, such that one or more flits of the second cache line is sent between two consecutive flits of the first cache line.

20. (Original) The system of claim 19, wherein the memory controller sends the interleaved flits in two packets.

21. (Original) The system of claim 20, wherein the multiplexer time-multiplexes the first and the second pluralities of flits in a plurality of time slots to interleave the first and second pluralities of flits.

22. (Original) The system of claim 21, wherein the multiplexer dynamically time-multiplexes the first and the second pluralities of flits.

23. (Original) The system of claim 21, wherein the multiplexer statically time-multiplexes the first and the second pluralities of flits.

24. (Original) The system of claim 20, further comprising a packetized interconnect coupled to the memory controller to send the interleaved flits.

25. (Original) The system of claim 19, wherein a critical chunk of each of the first and second read data returns is sent in one or more flits.

26. (Original) The system of claim 19, wherein the memory controller receives the first and second read data returns in a substantially overlapped manner.

27. (Original) The system of claim 19, further comprising a processor coupled to the memory controller to receive the interleaved flits of the first and second cache lines.

28. (Original) The system of claim 27, wherein the processor comprises a demultiplexer to separate the flits received.

29. (Original) The system of claim 19, further comprising:

a third plurality of DRAM devices; and

a third DRAM channel coupled to the third plurality of DRAM devices and the memory controller, wherein the memory controller further includes:

a third buffer, coupled to the multiplexer, to temporarily hold a third cache line of a third read data return from the third DRAM channel, wherein the

multiplexer interleaves a third plurality of flits of the third cache line with the first and second pluralities of flits.

30. (Original) The system of claim 29, further comprising:

a fourth plurality of DRAM devices; and

a fourth DRAM channel coupled to the fourth plurality of DRAM devices and the memory controller, wherein the memory controller further includes:

a fourth buffer, coupled to the multiplexer, to temporarily hold a fourth cache line of a fourth read data return from the fourth DRAM channel, wherein the multiplexer interleaves a fourth plurality of flits of the fourth cache line with the first, the second, and the third pluralities of flits.

31. (Currently amended) A method comprising:

interleaving a first plurality of flits containing a first critical chunk of ~~each of~~ a first cache line and a second plurality of flits containing a second critical chunk of a second cache ~~lines~~ line, the first and second pluralities of flits corresponding to a first and a second read data returns, respectively, such that one or more flits of the second plurality of flits are between two consecutive flits of the first plurality of flits;

sending the interleaved flits; and

sending a ~~second~~ third plurality of flits containing the first cache line's non-critical chunks after the interleaved flits are sent.

32. (Currently amended) The method of claim 31, further comprising:

sending a ~~third~~ fourth plurality of flits containing the second cache line's non-critical chunks after the ~~second~~ third plurality of flits are sent.

33. (Original) The method of claim 32, wherein the first and second read data returns are from a first and a second memory channels, respectively.

34. (Original) The method of claim 31, further comprising:

receiving the first and the second read data returns in a substantially overlapped manner.

35. (Currently amended) A method comprising:

interleaving a plurality of flits containing a critical chunk of each of a first, a second, and a third cache lines corresponding to a first, a second, and a third read data returns, respectively, into a stream of flits such that alternating flits in the stream are from a different cache line;

sending the interleaved flits; and

sending a second plurality of flits containing the first cache line's non-critical chunks after the interleaved flits are sent.

36. (Original) The method of claim 35, further comprising:

sending a third plurality of flits containing the second cache line's non-critical chunks after the second plurality of flits are sent; and

sending a fourth plurality of flits containing the third cache line's non-critical chunks after the third plurality of flits are sent.

37. (Original) The method of claim 36, wherein the first, the second, and the third read data returns are from a first, a second, and a third memory channels, respectively.

38. (Original) The method of claim 35, further comprising:

receiving the first, the second, and the third read data returns in a substantially overlapped manner.

39. (Currently amended) A method comprising:

interleaving a plurality of flits containing a critical chunk of each of a first, a second, a third, and a fourth cache lines corresponding to a first, a second, a third and a fourth read data returns, respectively, into a stream of flits such that alternating flits in the stream are from a different cache line;

sending the interleaved flits; and

sending a second plurality of flits containing the first cache line's non-critical chunks after the interleaved flits are sent.

40. (Original) The method of claim 39, further comprising:

sending a third plurality of flits containing the second cache line's non-critical chunks after the second plurality of flits are sent;

sending a fourth plurality of flits containing the third cache line's non-critical chunks after the third plurality of flits are sent; and

sending a fifth plurality of flits containing the fourth cache line's non-critical chunks after the fourth plurality of flits are sent.

41. (Original) The method of claim 40, wherein the first, the second, the third, and the fourth read data returns are from a first, a second, a third, and a fourth memory channels, respectively.

42. (Original) The method of claim 39, further comprising:

receiving the first, the second, the third, and the fourth read data returns in a substantially overlapped manner.

43. (Currently amended) A method comprising:

checking whether a buffer in a memory controller holds a critical chunk of a cache line of an oldest read return in a queue;

sending the critical chunk from the memory controller to a processor coupled to the memory controller if the buffer holds the critical chunk;

checking whether a predetermined number of non-critical chunks of the cache line have accumulated in the buffer after the critical chunk is sent; and

interleaving flits of the non-critical chunks with a plurality of flits of a second cache line at the memory controller; and

~~sending the non-critical chunks~~ if the predetermined number of non-critical chunks have accumulated in the buffer, sending the interleaved flits of the non-critical chunks from the memory controller to the processor.

44. (Original) The method of claim 43, further comprising:

removing the oldest read return from the queue after sending the non-critical chunks.

45. (Original) The method of claim 44, wherein the critical chunk and the non-critical chunks are sent via a packetized interconnect.